SYLLABUS

1. **Course name:** Digital IC Design Using HDL
2. **Course code:** DSIC330563
3. **Credits:** 3 (3/0/6)
   Duration: 15 weeks (45h main course and 90h self-study)
4. **Instructors:**
   1- Nguyen Dinh Phu, MEng
   2- Nguyen Tan Nhu, MEng
5. **Course conditions**
   Prerequisites: Digital Systems
   Corequisites: Digital Systems
6. **Course description**

This course provides students the knowledge of some device technologies and how to apply the HDL to describe basic circuits in Digital Systems. The basic device technologies taught in this course include ASIC, FPGA, and PLD. The Very High Speed Hardware Description Language (VHDL) is applied to design combinational circuits, sequential circuits in digital systems. After acquired the basic structures of IC design in VHDL, the tasks are developed to the higher level by concentrating to the optimization of timing and resources in order to get the suitable required performance of the IC circuits. The two main optimization methods being provided to students are operating sharing and functionality sharing. Moreover, the Finite State Machine (FSM) model is provided to design large sequential digital systems using VHDL. Finally, students are able to use the simulation software supported by Xilinx and Altera co-operations to verify the functions of designed IC circuits.

7. **Course Goals**

Goals	***Goal description*** *(This course provides students:)*	**ELOs**
G1	Basic knowledge of the VHDL in digital IC design	01 (H)
G2	An ability to use English in reading and writing technological documents	05 (M)
G3	An ability to analyze, calculate, explain, and resolve the problems related to the optimization of delay timing, resources, and performance in digital IC design	07 (M)
G4	An ability to design and simulated the digital circuits using VHDL	02 (M)

** Note: High: H; Medium: M; Low: L*

8. **Course Learning Outcomes (CLOs)**

CLOs		***Description*** *(After completing this course, students can have:)*	**Outcome**
G1	G1.1	The ability to discriminate device technologies, design levels, and	01

		design flows in digital IC design using HDL	07
	G1.2	The ability to discriminate and apply various design structures of VHDL	
	G1.3	The ability to use the concurrent signal assignment statements of VHDL	01 07
	G1.4	The ability to use the sequential signal assignment statements of VHDL	01 07
G2	G2.1	The ability to understand the datasheets of PAL, GAL, the training courses, the slides, and the technological terms in English	05 07
	G2.2	The ability to use English in answering the assignment tests	
G3	G3.1	The ability to calculate resources and delay of digital systems based on the analyzing of operators and structures described in VHDL	01, 02, 07
	G3.2	The ability to optimize digital systems in delay and resources by using operator sharing and functionality sharing techniques	01, 02, 07
G4	G4.1	The ability to use the EAD software supported by Xilinx and Altera to design and simulate the digital circuits described by VHDL	02

9. Study materials

- Textbooks:

[1] Pong P. Chu, *RTL Hardware Design Using VHDL*, A John Wilay & Sons Inc. Publication, 2006.

- References:

[2] Nguyen Dinh Phu, *the lessons of Digital IC Design Using VHDL*, HCM City University of Technology and Education, 2016.

10. Sudent Assessments

- Grading points: 10

- Planning for students assessment is followed:

Type	Contents	Linetime	Assessment techniques	CLOs	Rates (%)
Midterms					**30**
Exam01	Combinational circuit designs	Week 9	Individual paper assessment in class	G1.2 G1.3 G1.4 G2.2	15
Exam02	Sequential circuit designs	Week 12	Individual paper assessment in class	G1.2 G1.3 G1.4 G2.2	15
Frequent assignments in the online learning systems					**10**
Test 1	The overviews of digital systems and hardware description languages	Week 2, Week 4	Quizes	G1.1 G1.2 G2.2	5

Test 2	The signal assigment statements, synthesis flows, and design flows in digital IC design using VHDL	Week 6, Week 8, Week 10	Quizes	G1.2 G1.3 G1.4 G2.2	5
Big Projects					**10**
Project 1	Design, verify, and simulate the combincational circuits described in VHDL	Week 8	Reports	G1.2 G1.3 G1.4 G2.1 G4.1	5
Project 2	Design, verify, and simulate the sequential circuits described in VHDL	Week 13	Reports	G1.2 G1.3 G1.4 G2.1 G3.1 G3.2 G4.1	5
Final exam					**50**
Final Exam	The contents are covered all remaining outcomes of the course. The time length is 90 minutes.		Individual paper assessment in class	G2.2 G3.1 G3.2	50

11. Course details:

Weeks	Contents	CLOs
1	***Chapter 1:*** **< INTRODUCTION TO THE DIGITAL SYSTEMS>** *(3/0/6)*	
	A/ **Contents and teaching methods***: (2)* **Contents:** 1.1 Introduction 1.2 Device technologies 1.3 System representations 1.4 Levels of abstraction 1.5 EDA softwares 1.6 IC design flows **Teaching methods**: + Presentation + Questioning	G1.1 G2.1
	B/ **Self-study contents**: *(4)* 1.7 Homework	G2.2
2	***Chapter 2: <INTRODUCTION TO THE HARDWARE DESCIPTION LANGUAGES> (3/0/6)***	

	A/* Contents and teaching methods: (2)* **Contents:** 2.1 Hardware description languages 2.2 Basic concepts of VHDL **Teaching methods**: + Presentation + Questioning	G1.2 G1.3 G2.1
	***B/* Self-study contents**: *(4)* 2.3 Homework	G2.2
3, 4	***Chapter 3:* < BASIC STRUCTURES OF VHDL >** *(9/0/18)*	
	A/* Contents and teaching methods:(2)* **Contents:** 3.1 Introduction 3.2 Units and general formats of a VHDL program 3.3 Objects 3.4 Data types and operators 3.5 Pre-defined data types in VHDL 3.6 Data operators for array data types 3.7 Data types in the IEEE package 3.8 std_logic packaga 3.9 Comment in VHDL **Teaching methods**: + Presentation + Questioning	G1.1 G1.2 G2.1
	***B/* Self- study contents**: *(4)* 3.10 Homework	G2.2
5, 6	***Chapter 4:* < CONCURRENT SIGNAL ASSIGNMENT STATEMENTS IN VHDL >** *(9/0/18)*	
	A/* Contents and teaching methods: (2)* **Contents:** 4.1 Discriminate between the combinational and sequential circuits 4.2 The simple signal assigment statement 4.3 The conditional signal assignment statement 4.4 The selected signal assignment statement 4.5 Comparision between the conditional and selected signal assignment statements **Teaching methods**: + Presentation + Questioning + Discussion	G1.3 G2.1
	***B/* Self- study contents**: *(4)* 4.6 Homework	G2.2

7	***Chapter 5:*** **< SEQUENTIAL SIGNAL ASSIGNMENT STATEMENTS IN VHDL >** *(9/0/18)*	
	A/ **Contents and teaching methods***: (2)* **Contents:** 5.1 Process in VHDL 5.2 Sequential signal assignment statements 5.3 The variable assignment statements 5.4 the if statement 5.5 the case statement 5.6 Simple Loop statements 5.7 The synthesis of senquential statements **Teaching methods**: + Presentation + Questioning + Discussion	G1.1 G1.3 G2.1
	B/ **Self- study contents**: *(4)* 5.8 Homework	G2.2
8, 9	***Chapter 6:*** **<THE SYNTHESIS OF VHDL CODES>** *(9/0/18)*	
	A/ **Contents and teaching methods***: (2)* **Contents:** 6.1 Basic limitations of EDA softwares 6.2 Operator realization in VHDL 6.3 Usage of the 'Z' value in the std_logic data_type in VHDL 6.4 The synthesis flow of VHDL codes 6.5 Timing consideration 6.6 Simple Loop statements **Teaching methods**: + Presentation + Discussion	G3.1 G2.1
	B/ **Self- study contents**: *(4)* 6.7 Homework	G2.2
10, 11	***Chapter 7:*** **< COMBINATIONAL CIRCUITS >** *(9/0/18)*	
	A/ **Contents and teaching methods***: (2)* **Contents:** 7.1 Main principles to design the high performance logic circuits 7.2 Operator sharing 7.3 Funcionality sharing 7.4 Layout-related circuits 7.5 General examples **Teaching methods**: + Presentation + Questioning	G3.1 G3.2 G2.1

	+ Discussion	
	***B/* Self- study contents**: *(4)* 7.6 Homework	G2.2
12, 13	***Chapter 8:* <BASIC SEQUENTIAL CIRCUIT DESIGNS>** *(9/0/18)*	
	A/* Contents and teaching methods: (2)* **Contents:** 8.1 Overviews of sequential circutis 8.2 Synchronous circuits 8.3 Danger of synthesizing asynchronous circuits 8.4 Basic memorizing elements 8.5 Basic examples 8.6 Timing analysis in synchronous circuits 8.7 Using variables in sequential circuit descriptions 8.8 Synthesis of sequential circuits **Teaching methods**: + Presentation + Questioning	G1.1 G1.2 G2.1 G3.2 G4.1
	***B/* Self- study contents**: *(4)* 8.9 Homework	G3.2 G4.1
14, 15	***Chapter 9:* <FINITE STATE MACHINE (FSM)>** *(9/0/18)*	
	A/* Contents and teaching methods: (3)* **Contents:** 9.1 Overview 9.2 FSM representation 9.3 Timing and performance of an FSM 9.4 Moore machine versus Mealy machine 9.5 VHDL desciption of FSMs 9.6 State assigment 9.7 Moore output buffering 9.8 FSM design examples **Teaching methods**: + Presentation + Questioning + Discussion	G1.2 G2.1 G3.2 G4.1
	***B/* Self- study contents**: *(6)* 9.9 Homework	G4.1

12. Learning ethics:

- Home assignments and projects must be done by the students themselves. Plagiarism found in the assessments will get zero point

13. First approved date: August 01 2012

14. Approval level:

Dean	Department	Instructor

15. Syllabus updated process

1st time: Updated content dated **2st time:** Updated content dated	Instructors Nguyen Dinh Phu Head of department